# Intel® High Definition Audio Specification
## Document Change Notification


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Change Identification: **DCN No: HDA017-A**
Document Revision: Intel® High Definition Audio 1.0



## Title: Clarification of CORB & RIRB Size Read/Write requirement

### Brief description of the functional changes:

The definition in the HD Audio specification requires that the CORBSIZE and RIRBSIZE fields of the CORB & RIRB size registers be Read/Write, even though the controller is only required to support one size. When only one size is implemented, then the capability to write the size register is not possible.

## Current Definitions:

### 3.3.24 Offset 4Eh: CORBSIZE – CORB Size

Length: 1 byte

**Table 1. CORB Size**

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7:4</td><td>RO</td><td>Imp.Dep</td><td>CORB Size Capability (CORBSZCAP): A bit mask indicating the sizes of the CORB supported by the controller.
<table>
<tr><th>Bits [7:4]</th><th>CORB Size</th></tr>
<tr><td>0001</td><td>8 B = 2 entries</td></tr>
<tr><td>0010</td><td>64 B = 16 entries</td></tr>
<tr><td>0100</td><td>1024 B = 256 Entries</td></tr>
<tr><td>1000</td><td>Reserved</td></tr>
</table>
This is implemented as a bit mask; for example, if the controller supported two entries and 256 entries, this register would have a value of 0101b.</td></tr>
<tr><td>3:2</td><td>RsvdP</td><td>0</td><td>Reserved</td></tr>
</table>

| Bit | Type | Reset | Description |
|---|---|---|---|
| 1:0 | RW | Imp.Dep | **CORB Size (CORBSIZE):** The setting of the register determines when the address counter in the DMA controller will wrap around.<br>Bits [1:0] / CORB Size<br>00 / 8 B = 2 entries<br>01 / 64 B = 16 entries<br>10 / 1 KB = 256 entries<br>11 / *Reserved* |

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### 3.3.31 Offset 5Eh: RIRBSIZE – RIRB Size

Length: 1 byte

**Table 2. RIRB Size**

| Bit | Type | Reset | Description |
|---|---|---|---|
| 7:4 | RO | Imp.Dep | **RIRB Size Capability (RIRBSZCAP):**<br>A bit mask identifying the possible sizes of the RIRB.<br>Bits [7:4] / RIRB Size<br>0001 / 16 B = 2 entries<br>0010 / 128 B = 16 entries<br>0100 / 2048 B = 256 Entries<br>1000 / *Reserved*<br>This implemented as a bit mask; for example, if the controller supported two entries and 256 entries, this register would be Read Only 0101b. |
| 3:2 | RsvdP | 0 | *Reserved* |
| 1:0 | RW | Imp.Dep | **RIRB Size (RIRBSIZE):** The setting of the register determines when the address counter in the DMA controller will wrap around.<br>Bits [1:0] / RIRB Size<br>00 / 16 B = 2 entries<br>01 / 128 B = 16 entries<br>10 / 2 KB = 256 entries<br>11 / *Reserved*<br>This value must not be changed when the RIRB DMA engine is enabled. |

## New Definition:

### 3.3.24 Offset 4Eh: CORBSIZE – CORB Size

Length: 1 byte

**Table 3. CORB Size**

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7:4</td><td>RO</td><td>Imp.Dep</td><td>CORB Size Capability (CORBSZCAP): A bit mask indicating the sizes of the CORB supported by the controller.
<table>
<tr><th>Bits [7:4]</th><th>CORB Size</th></tr>
<tr><td>0001</td><td>8 B = 2 entries</td></tr>
<tr><td>0010</td><td>64 B = 16 entries</td></tr>
<tr><td>0100</td><td>1024 B = 256 Entries</td></tr>
<tr><td>1000</td><td>Reserved</td></tr>
</table>
This is implemented as a bit mask; for example, if the controller supported two entries and 256 entries, this register would have a value of 0101b.<br><br>There is no requirement to support more than one CORB Size.</td></tr>
<tr><td>3:2</td><td>RsvdP</td><td>0</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>RW or RO if only one size supported</td><td>Imp.Dep</td><td>CORB Size (CORBSIZE): The setting of the register determines when the address counter in the DMA controller will wrap around.
<table>
<tr><th>Bits [1:0]</th><th>CORB Size</th></tr>
<tr><td>00</td><td>8 B = 2 entries</td></tr>
<tr><td>01</td><td>64 B = 16 entries</td></tr>
<tr><td>10</td><td>1 KB = 256 entries</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
Setting this field to an unsupported size will produce unspecified results. When only one CORB Size is supported it is permissible to make this field Read Only (RO).</td></tr>
</table>

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### 3.3.31 Offset 5Eh: RIRBSIZE – RIRB Size

Length: 1 byte

**Table 4. RIRB Size**

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7:4</td><td>RO</td><td>Imp.Dep</td><td>RIRB Size Capability (RIRBSZCAP):<br>A bit mask identifying the possible sizes of the RIRB.<br><table><tr><th>Bits [7:4]</th><th>RIRB Size</th></tr><tr><td>0001</td><td>16 B = 2 entries</td></tr><tr><td>0010</td><td>128 B = 16 entries</td></tr><tr><td>0100</td><td>2048 B = 256 Entries</td></tr><tr><td>1000</td><td>Reserved</td></tr></table>This implemented as a bit mask; for example, if the controller supported two entries and 256 entries, this register would be Read Only 0101b.<br><br>There is no requirement to support more than one RIRB Size.</td></tr>
<tr><td>3:2</td><td>RsvdP</td><td>0</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>RW</td><td>Imp.Dep</td><td>RIRB Size (RIRBSIZE): The setting of the register determines when the address counter in the DMA controller will wrap around.<br><table><tr><th>Bits [1:0]</th><th>RIRB Size</th></tr><tr><td>00</td><td>16 B = 2 entries</td></tr><tr><td>01</td><td>128 B = 16 entries</td></tr><tr><td>10</td><td>2 KB = 256 entries</td></tr><tr><td>11</td><td>Reserved</td></tr></table>This value must not be changed when the RIRB DMA engine is enabled.<br><br>Setting this field to an unsupported size will produce unspecified results. When only one RIRB Size is supported it is permissible to make this field Read Only (RO).</td></tr>
</table>